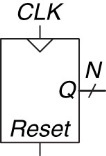
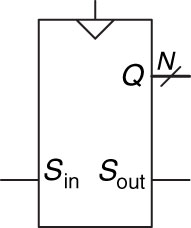
What is the Difference between Sequential and Combinational Logic Circuits?



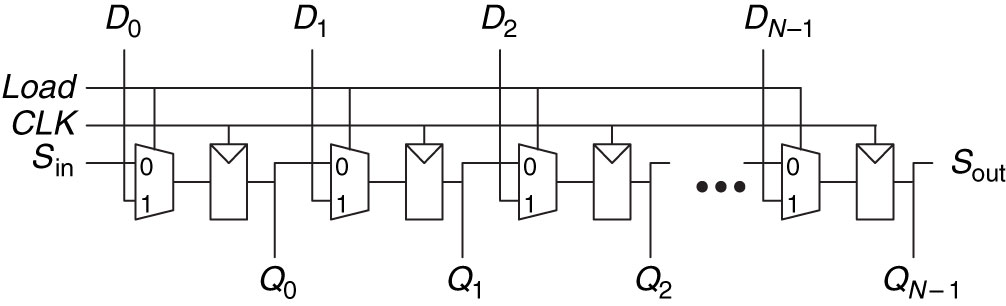
*Counter:*



Flip-Flop –

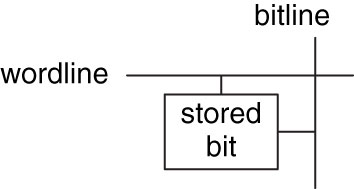
*Shift Register:*





What is the difference between a Shifter and a Shift Register?

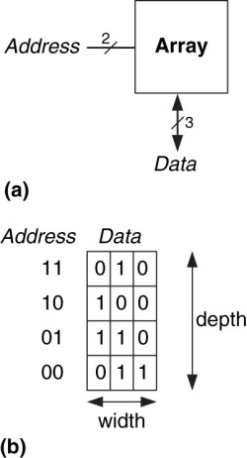


Memory

* **Address – Indicates which \_\_\_\_\_\_\_\_ of \_\_\_\_\_\_\_\_ is read/written (location) \_\_\_\_\_ (\_\_\_-Bits)**
* **Data – \_\_\_\_\_\_\_\_ read/written (\_\_\_-Bits)**
* **Word – \_\_\_\_\_\_\_\_ of a \_\_\_\_\_\_\_\_ of \_\_\_\_\_\_\_\_ (\_\_\_-Bits)**
* **Depth – Number of \_\_\_\_\_\_\_\_**
* **Width – Number of \_\_\_\_\_\_\_\_**
* **Wordline – \_\_\_\_\_\_\_\_ based on \_\_\_\_\_\_\_\_ to activate bit cells in a \_\_\_\_\_\_\_\_**
* **Bitline – kept at \_\_\_\_; when \_\_\_\_\_\_\_\_\_\_\_ is activated, driven to 1 or 0 by bit cell to \_\_\_\_\_\_\_\_**
  + **When written , drives bit cell high or low**
* **Port – Gives \_\_\_\_\_\_\_\_ /\_\_\_\_\_\_\_\_ access to the \_\_\_\_\_\_\_\_; multi-ported can read/write several \_\_\_\_\_\_\_\_\_\_ at the same time**

Address –

Data –

Word –

Depth -

Width –

Wordline –

Bitline –

Port –

**RAM – Random Access Memory**

* + - **Delay \_\_\_\_\_\_\_ for all \_\_\_\_\_\_\_, vs sequential (e.g. type)**
    - **\_\_\_\_\_\_\_ – \_\_\_\_\_\_\_ its data when the power is lost**

**ROM – Read Only Memory**

* + - **Also \_\_\_\_\_\_\_\_\_\_ accessed**
    - **Many can be \_\_\_\_\_\_\_ now**
    - **\_\_\_\_\_\_\_ -\_\_\_\_\_\_\_**

**Types of memory:**

**RAM – \_\_\_\_\_\_\_\_ \_\_\_\_\_\_\_ Memory**

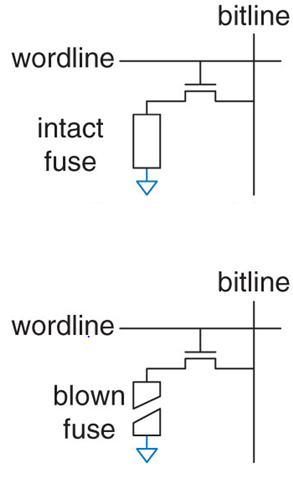
**ROM – \_\_\_\_\_\_\_\_ \_\_\_\_\_\_\_ Memory**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| ***Types of RAM:***  **DRAM –**  **DRAM – Dynamic RAM**   * + **Bit stored as \_\_\_\_\_\_\_\_ or \_\_\_\_\_\_\_\_ of \_\_\_\_\_\_\_\_ on a capacitor**   + **Reading \_\_\_\_\_\_\_\_ data; must be rewritten**   + **Must be \_\_\_\_\_\_\_\_ every few miliseconds due to leaking charge**   **SRAM –**  **SRAM – Static RAM**   * + **Does not need \_\_\_\_\_\_\_\_\_\_\_**   + **Bit stored in \_\_\_\_\_\_\_\_ \_\_\_\_\_\_\_\_ inverters**   + **Inverters can restore value if \_\_\_\_\_\_\_\_ \_\_\_\_\_\_\_\_** | ***Types of DRAM:***  **SDRAM –**  **SDRAM – \_\_\_\_\_\_\_\_\_\_\_\_\_ DRAM**   * + - **Uses \_\_\_\_\_\_\_\_\_\_\_\_ memory access**   **DDR SDRAM – \_\_\_\_\_\_\_\_ \_\_\_\_\_ \_\_\_\_\_ SDRAM**   * + - **Uses \_\_\_\_\_ and \_\_\_\_\_ edge to access data**   **DDR SDRAM –**   |  |  |  | | --- | --- | --- | | **Memory Type** | **Transistors per bit cell** | **Latency** | |  |  |  | |  |  |  | |  |  |  | |

**Register file -**

**Register File – \_\_\_\_\_\_\_\_ of registers that \_\_\_\_\_\_\_\_ temporary \_\_\_\_\_\_\_\_**

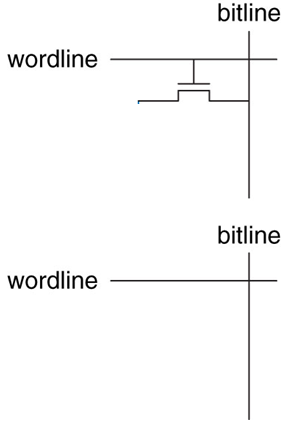
* + **Often consists of small \_\_\_\_\_\_\_\_\_\_\_\_\_\_ \_\_\_\_\_\_\_\_**

*Types of ROM:*

**PROM – \_\_\_\_\_\_\_\_\_\_ \_\_\_\_\_\_\_\_ \_\_\_\_\_\_\_\_ Memory– Provides a way to connect transistor with \_\_\_\_\_\_\_**

**PROM**

**Fuse Programmable ROM**

PROM –

**\_\_\_\_\_\_\_\_ \_\_\_\_\_\_\_\_\_\_\_\_\_\_ ROM – \_\_\_\_\_ \_\_\_\_\_ = 1, cannot be rewritten**

Fuse-programmable ROM –

**EPROM – \_\_\_\_\_\_\_\_\_\_\_\_ PROM**

* + **High voltage to \_\_\_\_\_\_\_\_**
  + **\_\_\_\_\_ \_\_\_\_\_\_\_\_ to erase**

EPROM –

**EEPROM – \_\_\_\_\_\_\_\_\_\_\_\_ EPROM**

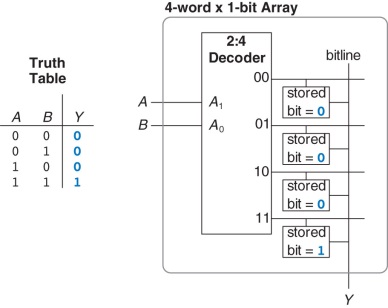
* + **Bit cells \_\_\_\_\_\_\_\_\_\_\_ erased**
  + **Erased without UV light with extra circuitry**

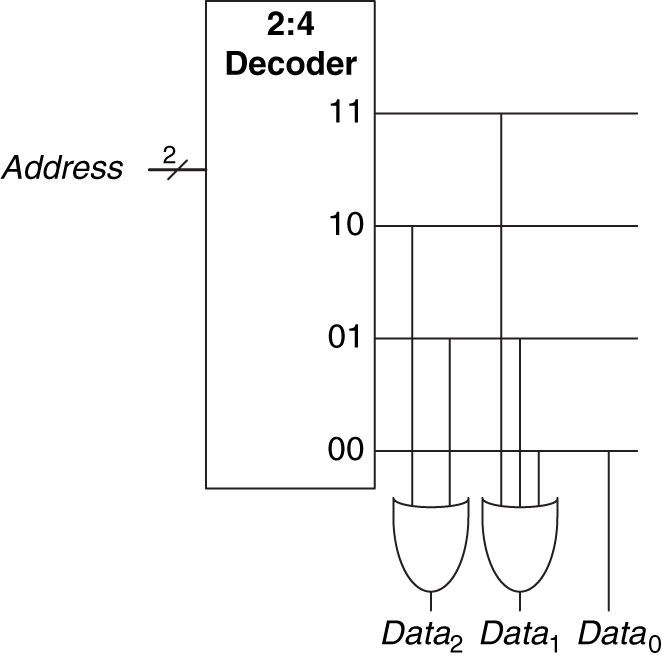
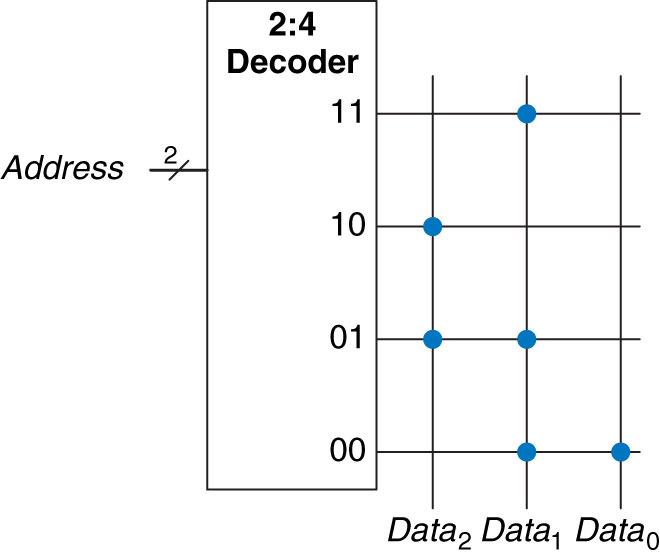
EEPROM –

**Flash – \_\_\_\_\_\_\_\_ \_\_\_\_\_\_\_\_ \_\_\_\_\_\_\_\_**

* + **Cheaper because less \_\_\_\_\_\_\_\_ circuitry**

Flash –

Logic using memory arrays:

3 ROM Dot Notation with and without gates: